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1 Session 61: test response compaction and ATPG: Fault detection and diagnosis with parity trees for space compaction of test responses
Harald Vranken, Sandeep Kumar Goel, Andreas Glowatz, Juergen Schloeffel, Friedrich Hapke
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(683.19 KB) Additional Information: full citation, abstract, references, index terms

This paper shows that accurate fault detection and diagnosis are possible when applying a parity tree for space compaction of test responses and continuously observing the parity-tree output. We exploit that each set of faults results in a unique parity-tree output sequence that can be used as a unique fault signature for truly accurate fault detection and diagnosis. Our theoretical analysis shows that probabilities for fault cancellation and fault aliasing are extremely low and decrease with ci ...

Keywords: fault detection, fault diagnosis, test data compression

2 Session 61: test response compaction and ATPG: Test response compactor with programmable selector
Grzegorz Mrugalski, Janusz Rajski, Jerzy Tyszer
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(662.03 KB) Additional Information: full citation, abstract, references, index terms

The paper presents an efficient method for synthesis of scan chain selection logic. It is capable of acting as a flexible X-control logic for test response compactors. The same circuitry can also be employed to selectively gate scan chains for diagnostic purposes.

Keywords: VLSI test, compression, scan chain selection, unknown states

3 Session 61: test response compaction and ATPG: Unknown-tolerance analysis and test-quality control for test response compaction using space compactors
Mango C.-T. Chao, Kwang-Ting Cheng, Seongmoon Wang, Srimat Chakradhar, Wen-Long Wei
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press
Full text available: pdf(623.62 KB) Additional Information: full citation, abstract, references, index terms

For a space compactor, degradation of fault detection capability caused by the masking effects from unknown values is much more serious than that caused by error masking (i.e. aliasing). In this paper, we first propose a mathematical framework to estimate the percentage of observable responses under unknown-induced masking for a space compactor. We further develop a prediction scheme which can correlate the percentage of observable responses with the modeled-fault coverage and with a n-detection ...

Keywords: design for test, test response compaction

4 Session 60: bounded model checking and equivalence verification: Fast falsification based on symbolic bounded property checking
Prakash M. Peranandam, Pradeep K. Nalla, Jürgen Ruf, Roland J. Weiss, Thomas Kropf, Wolfgang Rosenstiel
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(877.68 KB) Additional Information: full citation, abstract, references, index terms

Symbolic property verification is an increasingly popular debugging method based on Binary Decision Diagrams (BDDs). The lack of optimization of the state space search is often responsible for the excessive growth of the BDDs. In this paper we present an accelerated symbolic property verification by means of a new *guiding* technique that automatically finds the set of interesting variables by exploiting the property and the transition relation of a design. Our property based state space gu ...

Keywords: fast falsification, guiding, property checking

5 Session 60: bounded model checking and equivalence verification: Transistor abstraction for the functional verification of FPGAs
Guy Dupenloup, Thierry Lemeunier, Roland Mayr
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(619.72 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses the use of transistor abstraction to enable the functional verification of FPGA fabrics with RTL models. It first describes the multiplexer structures that are used on a massive scale in FPGAs and the specific challenges that they pose to transistor abstraction tools. It then reviews previous approaches and shows that the cone model of the DESB system is particularly well suited to abstract FPGA logic because it makes pass-gate branches in multiplexer structures well apparen ...

Keywords: FPGA, cone model, functional verification, logic equivalence checking, multiplexer, register transfer level, transistor abstraction

6 Session 60: bounded model checking and equivalence verification: Early cutpoint insertion for high-level software vs. RTL formal combinational equivalence verification
Xiushan Feng, Alan J. Hu
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(566.16 KB) Additional Information: full citation, abstract, references, index terms

Ever-growing complexity is forcing design to move above RTL. For example, golden

functional models are being written as clearly as possible in software and not optimized or intended for synthesis. Thus, equivalence verification between the high-level software functional model and the RTL is needed. The typical approach is to convert the high-level software into RTL or gate-level hardware, via software path enumeration, symbolic execution, or high-level synthesis techniques, and then use hardware ...

Keywords: RTL, cutpoints, formal equivalence checking, software

7 Session 58: advanced methods for interconnect extraction, clocks and reliability: Reliability modeling and management in dynamic microprocessor-based systems

Eric Karl, David Blaauw, Dennis Sylvester, Trevor Mudge

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(714.20 KB) Additional Information: full citation, abstract, references, index terms

Reliability failure mechanisms, such as time dependent dielectric breakdown, electromigration, and thermal cycling have become a key concern in processor design. The traditional approach to reliability qualification assumes that the processor will operate at maximum performance continuously under worst case voltage and temperature conditions. However, the typical processor spends a very small fraction of its operational time at maximum voltage and temperature. In this paper, we show how this res ...

Keywords: dynamic reliability management, electromigration, modeling, oxide breakdown, thermal cycling

8 Session 58: advanced methods for interconnect extraction, clocks and reliability: Modeling and minimization of PMOS NBTI effect for robust nanometer design

Rakesh Vattikonda, Wenping Wang, Yu Cao

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(855.22 KB) Additional Information: full citation, abstract, references, index terms

Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this paper, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robus ...

Keywords: NBTI, performance degradation, reliability, temperature, threshold voltage, variability

9 Session 58: advanced methods for interconnect extraction, clocks and reliability: Clock buffer and wire sizing using sequential programming

Matthew R. Guthaus, Dennis Sylvester, Richard B. Brown

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(809.33 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates methods for clock skew minimization using buffer and wire sizing. First, a technique that significantly improves solution quality and stability of sequential programming-based buffer/wire sizing is used. Then, a new formulation of clock skew minimization that uses quadratic programming and considers sub-critical skews in addition

to the most critical skews is presented. The quality of results are verified to be more robust using Monte Carlo simulations to account for proc ...

Keywords: clock tree synthesis, robust design, skew

10 Session 57: new ideas in analog/RF modeling and simulation: Lookup table based simulation and statistical modeling of Sigma-Delta ADCs

Guo Yu, Peng Li

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(923.83 KB) Additional Information: full citation, abstract, references, index terms

Sigma-Delta (EΔ) ADCs have been widely adopted in data conversion applications due to the good performance. However, oversampling and complex circuit behavior render the simulation of these designs prohibitively time consuming. In this paper, a lookup table (LUT) based modeling technique is presented for efficient analysis of EΔ ADCs. In the proposed approach, various transistor-level circuit non-idealities are systematically characterized at the building-block level and the ...

Keywords: Sigma-Delta, lookup table, statistical modeling

11 Session 57: new ideas in analog/RF modeling and simulation: A robust envelope following method applicable to both non-autonomous and oscillatory circuits

Ting Mei, Jaijeet Roychowdhury

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(810.92 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we propose a novel envelope-following method which is uniformly applicable to both non-autonomous and oscillatory circuits. A key feature of our technique is the use of an efficient minimum least squares solution technique to solve an underdetermined envelope system directly. This leads to a general purpose approach which is much easier to solve than previous phase condition based envelope-following method, improving numerically robustness dramatically. We validate our method on a ...

Keywords: envelope following, least squares, phase condition

12 Session 57: new ideas in analog/RF modeling and simulation: Systematic development of nonlinear analog circuit macromodels through successive operator composition and nonlinear model decoupling

Ying Wei, Alex Doboli

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(665.70 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a systematic methodology for developing structural nonlinear macromodels for analog circuits. The methodology includes two steps: first, a nonlinear system is represented as a system with nonlinear inputs and linearly coupled blocks. Then, the linear couplings are removed. The methodology also uses a novel description of circuit nonlinearities as a successive composition of three operators. The generated nonlinear models are scalable, tunable according to the required accurac ...

Keywords: analog circuits, nonlinear macromodel, structural macromodel

13 Session 57: new ideas in analog/RF modeling and simulation: A multilevel technique for robust and efficient extraction of phase macromodels of digitally controlled oscillators

Xiaolue Lai, Jaijeet Roychowdhury

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(591.83 KB) Additional Information: full citation, abstract, references, index terms

PPV phase macromodels are important for speeding up simulation of oscillator related circuits, such as PLLs, without sacrificing accuracy. Prior numerical methods for extracting PPVs face very significant robustness and accuracy problems when confronted with digitally controlled oscillators (DCOs, core building blocks in digital phase-locked loops), due to large RC time-constants from gated capacitors. In this paper, we present a hierarchical harmonic balance based technique for numerically extr ...

Keywords: DCO, DPLL, PLL, PPV, VCO, macromodel, simulation

14 Session 56: beyond-the-die circuit and system integration: PELE: pre-emphasis & equalization link estimator to address the effects of signal integrity limitations

Wm. Bereza, Yuming Tao, Shoujun Wang, Tad Kwasniewski, Rakesh H. Patel

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, references, index terms

This paper discusses a methodology employed to create a tool that quantifies the effects of signal integrity limitations particularly for high-speed applications. The tool is based on a platform of routines which predict performance over high-speed links. It contains routines that optimize transmitter pre-emphasis and receiver equalization that lead to superior BER performance. The tool is qualified against Agilent's ADS simulator and correlated to measurements.

Keywords: analysis and optimization, layout, signal integrity, simulation beyond the die

15 Session 56: beyond-the-die circuit and system integration: System level signal and power integrity analysis methodology for system-in-package applications

Rohan Mandrekar, Krishna Bharath, Krishna Srinivasan, Ege Engin, Madhavan Swaminathan

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(773.55 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a methodology for performing system level signal and power integrity analyses of SiP-based systems. The paper briefly outlines some new modeling and simulation techniques that have been developed to enable the proposed methodology. Some results based on the application of this methodology on test systems are also presented.

Keywords: causality, finite difference method, modal decomposition, nodal admittance matrix method, power integrity, signal integrity, system-in-package (SiP)

16 Session 56: beyond-the-die circuit and system integration: Efficient escape routing for

hexagonal array of high density I/Os
Rui Shi, Chung-Kuan Cheng
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, index terms

The chip/package I/Os count has continuously been growing as the systems become more complicated. High density I/Os interconnection and efficient escape routing with high performance and low cost will greatly benefit the whole electronic system. We analyze the properties of the hexagonal array, which can hold about 15% more I/Os compared with the traditional square grid array. We propose three escape routing strategies for the hexagonal array: column-by-column horizontal escape routing, two-side ...

Keywords: BGA, escape routing, flip chip, hexagonal array

17 Session 56: beyond-the-die circuit and system integration: Exploring compromises among timing, power and temperature in three-dimensional integrated circuits
Hao Hua, Chris Mineo, Kory Schoenfliess, Ambarish Sule, Samson Melamed, Ravi Jenkal, W. Rhett Davis
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(1.00 MB) Additional Information: full citation, abstract, references, index terms

Three-dimensional integrated circuits (3DICs) have the potential to reduce interconnect lengths and improve digital system performance. However, heat removal is more difficult in 3DICs, and the higher temperatures increase delay and leakage power, potentially negating the performance improvement. Thermal vias can help to remove heat, but they create routing congestion, which also leads to longer interconnects. It is therefore very difficult to tell whether or not a particular system may benefit ...

Keywords: 3DIC, design flow, temperature dependency, trade off

18 Session 56: beyond-the-die circuit and system integration: A thermally-aware performance analysis of vertically integrated (3-D) processor-memory hierarchy
Gian Luca Loi, Banit Agrawal, Navin Srivastava, Sheng-Chih Lin, Timothy Sherwood, Kaustav Banerjee
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(1.57 MB) Additional Information: full citation, abstract, references, index terms

Three-dimensional (3-D) integrated circuits have emerged as promising candidates to overcome the interconnect bottlenecks of nanometer scale designs. While they offer several other advantages, it is expected that the benefits from this technology can potentially be off-set by thermal considerations which impact chip performance and reliability. The work presented in this paper is the first attempt to study the performance benefits of 3-D technology under the influence of such thermal constraints ...

Keywords: 3D ICs, VLSI, performance modeling, processor-memory, thermal analysis, three dimensional, vertical integration

19 Session 54: logic and sequential synthesis: Variability driven gate sizing for binning yield optimization
Azadeh Davoodi, Ankur Srivastava

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(678.53 KB) Additional Information: full citation, abstract, references, index terms

Process variations result in a considerable spread in the frequency of the fabricated chips. In high performance applications, those chips that fail to meet the nominal frequency after fabrication are either discarded or sold at a loss which is typically proportional to the degree of timing violation. The latter is called binning. In this paper we present a gate sizing-based algorithm that optimally minimizes the binning yield-loss. We make the following contributions: 1) prove the binning yield ...

Keywords: gate sizing, process variations, speed binning

20 Session 54: logic and sequential synthesis: Budgeting-free hierarchical design method for large scale and high-performance LSIs

Yuichi Nakamura, Mitsuru Tagata, Takumi Okamoto, Shigeyoshi Tawada, Ko Yoshikawa
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(653.98 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a new hierarchical design method for large scale and high-performance LSIs, which eliminates the need to perform budgeting. The budgeting step in hierarchical design partitions the total propagation time constraint for a path between any two flip-flops (FFs) in different hierarchical blocks into budgets for the different segments of the path that lie within different blocks. In practice, budgeting may result in the need for additional iterations of the synthesis and physical ...

Keywords: budgeting, hierarchical design, physical synthesis